Transition Capacitance and Diffusion Capacitance of Diode

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Transition Capacitance CT of Diode (Space Charge Capacitance)

With the increase of magnitude of reverse bias, majority carriers move away from the junction i.e. the width W of the depletion layer increases. These uncovered immobile charge on the two sides of the junction constitute a capacitor of incremental capacitance C_T given by,

$$C_T = |\frac{dQ}{dV}| \quad ....(1)$$

Where dQ is the increase in the charge resulting from an increase dV in voltage.

Hence, a voltage change dV in the time interval dt will result in a current i given by,

$$i = \frac{dQ}{dt} = C_T \frac{dV}{dt} \quad ....(2)$$

This capacitance C_T is called the transition capacitance or space charge capacitance or barrier capacitance or depletion layer capacitance.

C_T forms an important parameter of the junction. However, C_T varies with the magnitude of the reverse bias. More the magnitude of the reverse bias greater is the width W of the depletion layer and smaller is the transition capacitance C_T.

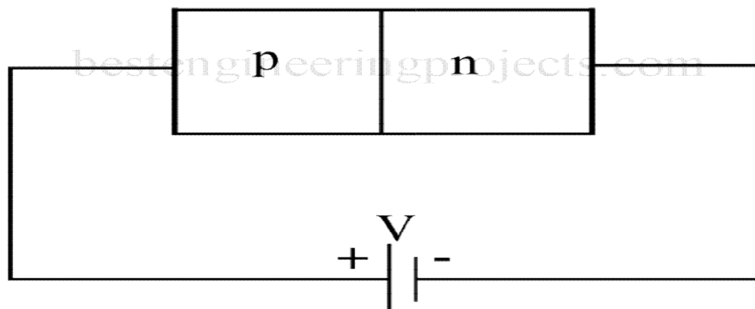

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Figure 2: Forward Biased PN Diode

C_T in a Step Graded Junction:

A junction is said to be step graded if there is an abrupt change from acceptor ion density on the P-side to donor ion density on the N-side. Such a junction gets formed in alloyed junction (or Fused Junction) diode. In general, the acceptor density N_A and the donor density N_D are kept unequal. The transition capacitance C_T is then given by,

$$C_T = \frac{\epsilon A}{W} \quad ....(3)$$

Where ϵ is a absolute permittivity of the semiconductor medium, A is the cross-sectional area of the junction and W is the of the depletion layer and is given by,

$$W^2 = [\frac{2\epsilon V_j}{q}][\frac{1}{N_A} + \frac{1}{N_D}] \quad ....(4)$$

In case $N_A >> N_D$,

$$W = (\frac{2\epsilon V_j}{N_D q})^{\frac{1}{2}} \quad ....(5)$$

Hence, $C_T = A(\frac{N_D}{\ldots})^{\frac{1}{2}} \times ($ ………(6)

Thus, in a step graded junction, C_T is inversely proportional to square root of junction voltage V_j where V_j is given by,

$V_j = V_o - V_d$ ………(7)

Where V_d is a negative number indicating the applied reverse bias and V_0 is the contact potential.

C_T in a Linear Graded Junction

A junction is said to be linear graded if there is a linear variation of net charge density with distance in the transition region. Such a junction gets formed in a frown junction diode.

In such a junction diode also, the transition capacitance is given by,

$C_T = \frac{\epsilon}{\ldots}$ ………..(8)

Thus, the expression for C_T for linearly graded junction is the same as for step graded junction.

However, in this case, assuming $N_A = N_D$, the width W of the depletion layer is given by,

$W = (\frac{6\epsilon V_j}{\ldots}$ ………(9)

Hence,

$C_T = A(\frac{N_D}{\ldots})^{\frac{1}{2}} \times ($ ……..(10)

Thus, in this case also, C_T is inversely proportional to the square root of V_j.

Diffusion Capacitance or Storage Capacitance C_D

In the forward biased diode, the potential barrier at the junction gets lowered. As a result, holes get injected from the P-side to the N-side and electron get injected from the N-side to the P-side. These injected charges get stored near the junction just outside the depletion layer, holes in the N-region and electrons in the P-region. Due to charge storage, the voltage lags behind the current producing the capacitance effect. Such a capacitance is called diffusion capacitance or storage capacitance C_D.

The diffusion capacitance C_D may be defined as the rate of change of injected charge with voltage,

Thus,

$C_D = \frac{d}{\ldots}$ ………..(11)

But, in a forward biased diode with one region say P-region very heavily doped relative to the other region (N region), current (I) is mainly due to holes. Then (I) is given by,

$I = \frac{(}{\ldots}$ …….(12)

Where Q is the stored charge and τ_p is the mean lifetime of hole and is given by,

$$T_p = \frac{I}{\tau}$$ …………(13)

Where L_P is the diffusion length for holes, and D_P is the diffusion constant for holes.

Combining Equation (11) and (12), we get

$$C_D = \tau \frac{dI}{dV} =$$ ………(14)

But from equation of dynamic resistance $r \approx \frac{\eta V}{I}$. Substituting this value of r in equation (14) we get,

$$C_D = \frac{\tau}{\eta I}$$ ………(15)

In a general case, diffusion constant C_D is caused by diffusion of both the holes in the n-regions and electrons in the P-region, resulting in diffusion capacitance C_{Dp} and C_{Dn} respectively. The total diffusion capacitance C_D is the sum of C_{Dp} and C_{Dn}.

C_D may have value of a few thousand of pF. This time constant C_D. r mainly limits the frequency response of certain semiconductor devices when used in high frequency applications.

In fact in a forward diode, there are present both the diffusion capacitance C_D and the transition capacitance C_T, but $C_D >> C_T$. Typically, C_D is more than a million times greater than C_T. Hence, in a forward biased diode, C_T may be neglected and we need consider only C_D.

Similarly, in reverse biased diode, these are present both C_D and C_T. But $C_D << C_T$. Hence, in a reverse biased diode, we may neglect C_D and we need consider only C_T.

For forward biased Ge diode $(\eta = 1)$, at $I = 13mA$, $r = 2\Omega$ and then $C_D = 0.5\tau$. For $\tau = 20\mu s$, $C_D = 10\mu F$.